In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown in accordance with the mandatory amendment format.

1. (Currently Amended) A method comprising:

receiving input data by an execution unit; **[[and]]**

performing, by the execution unit using a plurality of multiply-accumulate units in the execution unit, a plurality of current multiply-accumulate operations on the received input data; and

saving the received input data for one or more multiply-accumulate operations to be performed by the execution unit after the current multiply-accumulate operation;

wherein the performing a current multiply-accumulate operation includes:

multiplying the received input data with a multiplier in the execution unit;

adding an output from the multiplier with another value using an adder in the execution unit; and

storing an output of the adder and providing the another value to the adder using an accumulator in the execution unit; **[[and]]**

wherein the plurality of multiple-accumulate units are modular so that any number of multiply-accumulate units can be utilized proportionally for any given memory bandwidth ~~the performing is to implement a finite impulse response filter with the received input data comprising one or more tap coefficients and one or more input data samples and with accumulated data in the accumulator comprising one or more output data samples~~.

2. (Original) The method of claim 1, wherein the receiving comprises receiving

first and second data by the execution unit; and

wherein the performing comprises performing by the execution unit a multiply-accumulate operation on the received first and second data and a multiply-accumulate operation on the received first data and on input data saved by the execution unit.

3. (Original) The method of claim 1, wherein the receiving comprises receiving first, second, third, and fourth data by the execution unit; and

wherein the performing comprises performing by the execution unit a multiply-accumulate operation on the received first and third data, a multiply-accumulate operation on the received second and fourth data, a multiply-accumulate operation on the received first and fourth data, and a multiply-accumulate operation on the received second data and on input data saved by the execution unit.

4. (Original) The method of claim 3, wherein the performing the multiply-accumulate operation on the received first and third data and the multiply-accumulate operation on the received second and fourth data comprise multiplying the received first and third data to produce a first product, multiplying the received second and fourth data to produce a second product, and adding the first product, the second product, and an accumulated sum.

5. (Currently Amended) The method of claim 1, comprising:

~~saving by the execution unit received input data for one or more multiply-accumulate operations to be performed by the execution unit after the current multiply-accumulate operations;~~

repeating the receiving, performing, and saving by the execution unit one or more

times to accumulate data; and

outputting the accumulated data by the execution unit.

6. (Canceled)

7. (Previously Amended) The method of claim 1, wherein one or more tap coefficients are each a complex number and one or more input data samples are each a complex number.

8. (Original) The method of claim 1, comprising saving by the execution unit saved input data for one or more multiply-accumulate operations to be performed by the execution unit.

9. (Original) The method of claim 1, comprising performing the receiving and performing in accordance with a single instruction multiple data instruction.

10. (Currently Amended) An apparatus comprising:

an execution unit block having a plurality of inputs, the execution unit block comprising:

one or more buffers to save input data received at one or more of the inputs, the data to be utilized by the execution unit in a subsequent multiply-accumulate operations after current multiply-accumulate operations; [[,]] and

a plurality of multiplier-accumulators to perform multiply-accumulate operations, the multiplier-accumulators to perform the current multiply-accumulate operations on at least one of input data received at one or more of the inputs and prior input data received for one or more prior multiply-accumulate

operations that is stored in the one or more buffers; and[[,]]

a control logic block to control the multiplier-accumulators and the one or more buffers;

wherein each multiplier-accumulator includes a multiplier to multiply one or more input values, an adder to add an output from the multiplier with another value, and an accumulator to store an output from the adder and provide the another value to the adder, and

wherein the plurality of multiple-accumulators are modular so that any number of multiply-accumulators can be utilized proportionally for any given memory bandwidth ~~the multiplier-accumulators to perform the multiple-accumulate operations to implement a finite impulse response filter with the received input data comprising one or more tap coefficients and one or more input data samples and with accumulated data in the accumulator comprising one or more output data samples; and~~

~~control logic to control the multiplier-accumulators and the one or more buffers~~.

11. (Original) The apparatus of claim 10, the multiplier-accumulators to perform a multiply-accumulate operation on first and second input data received at the inputs and a multiply-accumulate operation on the received first input data and on input data stored in a buffer of the execution unit block.

12. (Original) The apparatus of claim 11, wherein the execution unit block comprises a single multiplier-accumulator comprising a multiplier to multiply the received first and second input data to produce a product, an accumulator to store an accumulated sum, and an adder to add the product to the accumulated sum.

13. (Original) The apparatus of claim 10, the multiplier-accumulators to perform a multiply-accumulate operation on first and third input data received at the inputs, a multiply-accumulate operation on second and fourth data received at the inputs, a multiply-accumulate operation on the received first and fourth data, and a multiply-accumulate operation on the received second data and on input data stored in a buffer of the execution unit block.

14. (Original) The apparatus of claim 13, wherein the execution unit block comprises a dual multiplier-accumulator comprising a multiplier to multiply the received first and third input data to produce a first product, a multiplier to multiply the received second and fourth input data to produce a second product, an accumulator to store an accumulated sum, and an adder to add the first product, the second product, and the accumulated sum.

15. (Original) The apparatus of claim 10, the execution unit block comprising one or more execution unit building blocks each comprising one or more multiplier-accumulators and one or more buffers.

16. (Original) The apparatus of claim 10, the control logic to control the execution unit block to repeat, one or more times, receiving input data at one or more of the inputs, performing multiply-accumulate operations on the received input data and on input data stored in one or more buffers of the execution unit block to accumulate data, and saving the received input data in one or more buffers of the execution unit block.

17. (Canceled)

18. (Previously Amended) The apparatus of claim 10, wherein the one or more tap coefficients are each a complex number and the one or more input data samples are each a complex number.

19. (Original) The apparatus of claim 10, the control logic to control the execution unit block to save input data stored in one or more buffers of the execution unit block for one or more multiply-accumulate operations to be performed by the execution unit block.

20. (Original) The apparatus of claim 10, the control logic to control the multiplier-accumulators and the one or more buffers in accordance with a single instruction multiple data instruction.

21. (Currently Amended) A system comprising:

a coder/decoder to receive analog signals and convert the analog signals into corresponding input data; and

a processor to process the corresponding input data, the processor including:

an execution unit block having a plurality of inputs, the execution unit block comprising:

one or more buffers to save input data received at one or more of the inputs, the data to be utilized by the execution unit in a subsequent multiply-accumulate operations after current multiply-accumulate operations; [[,]] and

a plurality of multiplier-accumulators to perform multiply-accumulate operations, the multiplier-accumulators to perform the current multiply-

accumulate operations on at least one of input data received at one or more of the inputs and prior input data received for one or more prior multiply-accumulate operations that is stored in the one or more buffers; and [[,]]

a control logic block to control the multiplier-accumulators and the one or more buffers;

wherein each multiplier-accumulator includes a multiplier to multiply one or more input values, an adder to add an output from the multiplier with another value, and an accumulator to store an output from the adder and provide the another value to the adder, and

wherein the plurality of multiple-accumulators are modular so that any number of multiply-accumulators can be utilized proportionally for any given memory bandwidth ~~the multiplier-accumulators to perform the multiple accumulate operations to implement a finite impulse response filter with the received input data comprising one or more tap coefficients and one or more input data samples and with accumulated data in the accumulator comprising one or more output data samples; and~~

~~control logic to control the multiplier-accumulators and the one or more buffers~~.

22. (Original) The system of claim 21, the multiplier-accumulators to perform a multiply-accumulate operation on first and second input data received at the inputs and a multiply-accumulate operation on the received first input data and on input data stored in a buffer of the execution unit block.

23. (Original) The system of claim 22, wherein the execution unit block

comprises a single multiplier-accumulator comprising a multiplier to multiply the received first and second input data to produce a product, an accumulator to store an accumulated sum, and an adder to add the product to the accumulated sum.

24. (Original) The system of claim 21, the multiplier-accumulators to perform a multiply-accumulate operation on first and third input data received at the inputs, a multiply-accumulate operation on second and fourth data received at the inputs, a multiply-accumulate operation on the received first and fourth data, and a multiply-accumulate operation on the received second data and on input data stored in a buffer of the execution unit block.

25. (Original) The system of claim 24, wherein the execution unit block comprises a dual multiplier-accumulator comprising a multiplier to multiply the received first and third input data to produce a first product, a multiplier to multiply the received second and fourth input data to produce a second product, an accumulator to store an accumulated sum, and an adder to add the first product, the second product, and the accumulated sum.

26. (Original) The system of claim 21, the execution unit block comprising one or more execution unit building blocks each comprising one or more multiplier-accumulators and one or more buffers.

27. (Original) The system of claim 21, the control logic to control the execution unit block to repeat, one or more times, receiving input data at one or more of the inputs, performing multiply- accumulate operations on the received input data and on input data stored in one or more buffers of the execution unit block to accumulate data, and saving

the received input data in one or more buffers of the execution unit block.

28. (Canceled)

29. (Original) The system of claim 21, the control logic to control the execution unit block to save input data stored in one or more buffers of the execution unit block for one or more multiply-accumulate operations to be performed by the execution unit block.

30. (Original) The system of claim 21, the control logic to control the multiplier-accumulators and the one or more buffers in accordance with a single instruction multiple data instruction.

31. (New) The method of claim 1, wherein the performing is to implement a finite impulse response filter with the received input data comprising one or more tap coefficients and one or more input data samples and with accumulated data in the accumulator comprising one or more output data samples.

32. (New) The apparatus of claim 10, wherein the multiplier-accumulators to perform the multiple accumulate operations to implement a finite impulse response filter with the received input data comprising one or more tap coefficients and one or more input data samples and with accumulated data in the accumulator comprising one or more output data samples.

33. (New) The system of claim 21, wherein the multiplier-accumulators to perform the multiple accumulate operations to implement a finite impulse response filter with the received input data comprising one or more tap coefficients and one or more input data

samples and with accumulated data in the accumulator comprising one or more output data samples.